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Evaluating the ADN8833 Ultracompact 1 A Thermoelectric Cooler (TEC) Controller Driver

FEATURES

Evaluation boards for the ADN8833
1.0 A TEC driver for digital control systems
Operating voltage range: V_{IN} = 2.7 V to 5.5 V
TEC voltage and current operation monitoring
Independent TEC heating and cooling current limit settings
Programmable maximum TEC voltage
External synchronization from 1.85 MHz to 3.25 MHz
Output for TEC module wires
2.5 V reference output
Disable jumper
40 mm × 25 mm WLCSP evaluation board size
45 mm × 25 mm LFCSP evaluation board size

DOCUMENTS NEEDED

ADN8833 data sheet

ADN8833CB-EVALZ AND ADN8833CP-EVALZ EVALUATION BOARDS

Figure 1. ADN8833CB-EVALZ WLCSP Evaluation Board

Figure 2. ADN8833CP-EVALZ LFCSP Evaluation Board

GENERAL DESCRIPTION

The ADN8833CB-EVALZ and ADN8833CP-EVALZ are configurable evaluation boards designed to work with various TEC modules. The ADN8833 on the evaluation board delivers bidirectional current through the TEC controller using two pairs of the complementary integrated MOSFETs in an H-bridge configuration.

The voltage across the TEC is proportional to the voltage of the control signal applied to the CONT input pin.

With the on-board passive components and TEC cooling and heating current limits set to 1 A, the maximum TEC voltage is programmed to 3 V. To modify the cooling and heating TEC current limits and maximum TEC voltage setting, change the values of the corresponding components.

TABLE OF CONTENTS

REVISION HISTORY

10/15—Revision 0: Initial Version

USING THE EVALUATION BOARD

BOARD CONNECTION

Apply a power source to the VIN (ADN8833CB-EVALZ)/VIN+ (ADN8833CP-EVALZ) and GND terminals. Connect the TEC module to TEC+ and TEC−. The power source voltage must not exceed 5.5 V, the maximum operation input voltage of the ADN8833. Apply the TEC driver control signal to the CONT terminal and AGND. Remove the shunt from the VLIM/SD jumper to enable the controller.

MAXIMUM TEC VOLTAGE

The maximum TEC cooling voltage is set to 3 V by the values of R_{V1} = 6.65 kΩ and R_{V2} = 10 kΩ.

To change the setting, modify the value of R_{V1} using the equations provided in the Using a Resistor Divider to Set the TEC Voltage Limit section (for more information, refer to the ADN8833 data sheet) or following the recommended values in Table 1.

Using a Resistor Divider to Set the TEC Voltage Limit

Calculate the cooling and heating limits using the following equations:

$$V_{VLIM\_COOLING} = V_{REF} \times R_{V2}/(R_{V1} + R_{V2})$$

where V_{REF} = 2.5 V.

$$V_{VLIM\_HEATING} = V_{VLIM\_COOLING} - I_{SINK\_VLIM} \times R_{V1}||R_{V2}$$

where I_{SINK_VLIM} = 10 µA.

$$V_{TEC\_MAX\_COOLING} = V_{VLIM\_COOLING} \times A_{VLIM}$$

where A_{VLIM} = 2 V/V.

$$V_{TEC\_MAX\_HEATING} = V_{VLIM\_HEATING} \times A_{VLIM}$$

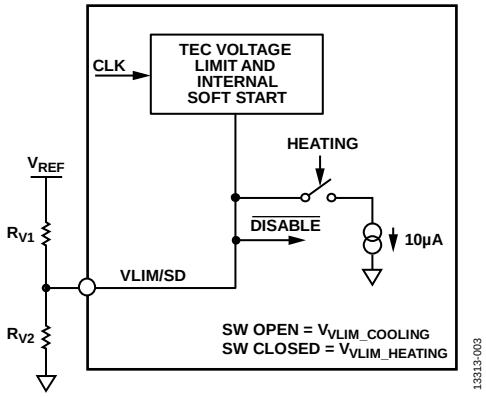

Figure 3. Programming the Maximum TEC Voltage

Table 1. Setting the Maximum TEC Voltage (R_{V2} = 10 kΩ)

$V_{TEC\_MAX\_COOLING}$ (V)[1]	$V_{VLIM\_COOLING}$ (V)[2]	R_{V1} (kΩ)[3]	$V_{TEC\_COOLING}$ (V)[4]	$R_{V1}\|\|R_{V2}$ (kΩ)[3]	$V_{VLIM\_HEATING}$ (V)[5]	$V_{TEC\_MAX\_HEATING}$ (V)[6]	$V_{TEC\_HEATING}$ (V)[7]
4.750	2.375	0.53	2.438	0.5	2.370	4.740	0.065
4.500	2.250	1.11	2.375	1.0	2.240	4.480	0.130
4.250	2.125	1.76	2.313	1.5	2.110	4.220	0.195
4.000	2.000	2.50	2.250	2.0	1.980	3.960	0.260
3.750	1.875	3.33	2.188	2.5	1.850	3.700	0.325
3.500	1.750	4.29	2.125	3.0	1.720	3.440	0.390
3.250	1.625	5.38	2.063	3.5	1.590	3.180	0.455
3.000	1.500	6.67	2.000	4.0	1.460	2.920	0.520
2.750	1.375	8.18	1.938	4.5	1.330	2.660	0.585
2.500	1.250	10.00	1.875	5.0	1.200	2.400	0.650
2.250	1.125	12.22	1.813	5.5	1.070	2.140	0.715
2.000	1.000	15.00	1.750	6.0	0.940	1.880	0.780
1.750	0.875	18.57	1.688	6.5	0.810	1.620	0.845
1.500	0.750	23.33	1.625	7.0	0.680	1.360	0.910
1.250	0.625	30.00	1.563	7.5	0.550	1.100	0.975
1.000	0.500	40.00	1.500	8.0	0.420	0.840	1.040
0.750	0.375	56.67	1.438	8.5	0.290	0.580	1.105
0.500	0.250	90.00	1.375	9.0	0.160	0.320	1.170
0.250	0.125	190.00	1.313	9.5	0.030	0.060	1.235

[1] $V_{TEC\_MAX\_COOLING}$ is the maximum target TEC voltage when the ADN8833 operates in cooling mode.
[2] $V_{VLIM\_COOLING}$ is the voltage set at the VLIM/SD input pin for cooling.
[3] R_{V1} is the required value of Resistor R1. R_{V2} is the required value of Resistor R2.
[4] $V_{TEC\_COOLING}$ is the voltage at the VTEC output when the TEC voltage reaches the maximum in cooling mode.
[5] $V_{VLIM\_HEATING}$ is the voltage set at the VLIM/SD input pin for heating.
[6] $V_{TEC\_MAX\_HEATING}$ is the maximum TEC voltage set when the ADN8833 operates in heating mode.
[7] $V_{TEC\_HEATING}$ is the voltage at the VTEC output when the TEC voltage reaches the maximum in heating mode.

COOLING AND HEATING TEC CURRENT LIMITS

The maximum TEC cooling and heating current limits are both set to 1 A by the values of R_{C1} = 90.9 kΩ and R_{C2} = 37.4 kΩ. To change the settings, use the equations provided in Using a Resistor Divider to Set the TEC Current Limit section (for more information, refer to the ADN8833 the data sheet) or use the values recommended in Table 3.

Using a Resistor Divider to Set the TEC Current Limit

The internal current sink circuitry connected to ILIM draws a 40 µA current when the ADN8833 drives the TEC in a cooling direction, which allows a high cooling current. Use the following equations to calculate the maximum TEC currents:

$$V_{ILIM\_HEATING} = V_{REF} \times R_{C2}/(R_{C1} + R_{C2})$$

where V_{REF} = 2.5 V.

$$V_{ILIM\_COOLING} = V_{ILIM\_HEATING} + I_{SINK\_ILIM} \times R_{C1}||R_{C2}$$

where I_{SINK_ILIM} = 40 µA.

$$I_{TEC\_MAX\_COOLING} = \frac{V_{ILIM\_COOLING} - 1.25\ \text{V}}{R_{CS}}$$

where R_{CS} = 0.525 V/A.

$$I_{TEC\_MAX\_HEATING} = \frac{1.25\ \text{V} - V_{ILIM\_HEATING}}{R_{CS}}$$

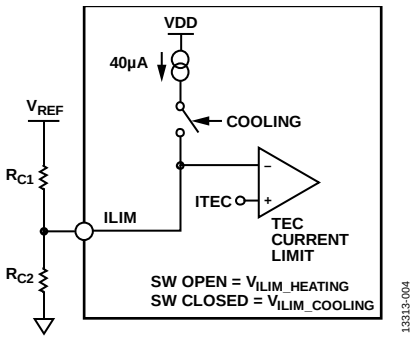

Figure 4. Programming the TEC Current Cooling and Heating Limits

PWM OPERATION FREQUENCY

The frequency of the PWM TEC driver stage can be configured at the 3-pin jumper, J1. Apply the external synchronization clock signal to the middle pin of the jumper.

Table 2. PWM Frequency Selection

EN/SY Pin	PWM Operation Frequency
Low (<0.8 V)	Shutdown
Open	Shutdown
High (>2.1 V)	2 MHz
External Clock Signal (High > 2.1 V, Low < 0.8 V)	From 1.85 MHz to 3.25 MHz

Table 3. Values of the Resistor Divider for ILIM Settings

$I_{TEC\_MAX\_COOLING}$ (A)[1]	$V_{ILIM\_COOLING}$ (V)[2]	$I_{TEC\_MAX\_HEATING}$ (A)[3]	$V_{ILIM\_HEATING}$ (V)[4]	R_{C1} (kΩ)[5]	R_{C2} (kΩ)[5]	$R_{C1}\|\|R_{C2}$ (kΩ)[5]
1.1	1.828	−1.1	0.673	107.3	39.5	28.875
1.0	1.775	−1.0	0.725	90.5	37.0	26.250
0.9	1.723	−0.9	0.778	76.0	34.3	23.625
0.8	1.670	−0.8	0.830	63.3	31.4	21.000
0.7	1.618	−0.7	0.883	52.1	28.4	18.375
0.6	1.565	−0.6	0.935	42.1	25.2	15.750
0.5	1.513	−0.5	0.988	33.2	21.7	13.125
0.4	1.460	−0.4	1.040	25.2	18.0	10.500
0.3	1.408	−0.3	1.093	18.0	14.0	7.875
0.2	1.355	−0.2	1.145	11.5	9.7	5.250
0.1	1.303	−0.1	1.198	5.5	5.0	2.625

[1] $I_{TEC\_MAX\_COOLING}$ is the maximum target TEC current when the ADN8833 operates in cooling mode
[2] $V_{ILIM\_COOLING}$ is the voltage set at the ILIM pin when the ADN8833 operates in cooling mode.
[3] $I_{TEC\_MAX\_HEATING}$ is the maximum target TEC current when the ADN8833 operates in heating mode.
[4] $V_{ILIM\_HEATING}$ is the voltage set at the ILIM pin when the ADN8833 operates in heating mode.
[5] R_{C1} is the required value of Resistor R3. R_{C2} is the required value of Resistor R4.

READ THE TEC VOLTAGE

The voltage on the VTEC output pin is proportional to the voltage across the TEC and is measured at Connector J5/Pin 1 (ADN8833CB-EVALZ, the WLCSP evaluation board) or J6/Pin 11 (ADN8833CP-EVALZ, the LFCSP evaluation board). The relationship between the voltage on the VTEC output and the voltage across the TEC is as follows:

$$V_{TEC} = V_{LDR} - V_{SFB} = 4 \times (V_{VTEC} - 0.5 \times V_{REF})$$

where:
V_{TEC} is the voltage across the TEC.
V_{LDR} is the voltage measured at the LDR pin.
V_{SFB} is the voltage measured at the SFB pin.
V_{VTEC} is the voltage measured at the VTEC pin.
V_{REF} is the reference voltage, 2.5 V.

READ THE TEC CURRENT

The voltage on the ITEC output pin is proportional to the TEC current, and is measured at Connector J5/Pin 2 (ADN8833CB-EVALZ) or J6/Pin 12 (ADN8833CP-EVALZ). Calculate the TEC current from the ITEC pin voltage as follows:

$$I_{TEC} = \frac{V_{ITEC} - 0.5 \times V_{REF}}{R_{CS}}$$

where:
I_{TEC} is the TEC current; defined as the current flowing into the TEC positive terminal TEC+ and out of the TEC negative terminal, TEC−.
V_{ITEC} is the voltage measured at the ITEC pin.
V_{REF} is the reference voltage, 2.5 V.
R_{CS} is the current sense gain, 0.525 V/A.

TEC DRIVER CONTROL

The TEC driver has a linear driver LDR and a PWM driver with an SW output and a voltage feedback input pin, SFB. It is controlled by the voltage signal at the CONT pin. The equations for the linear and PWM driver outputs, respectively, are as follows:

$$V_{LDR} = V_B - 40(V_{CONT} - 1.25\ \text{V})$$

$$V_{SFB} = V_{LDR} + 5(V_{CONT} - 1.25\ \text{V})$$

where:
V_{CONT} is the voltage at the CONT pin.
V_B is determined by the voltage at the VDD pin as

$$V_B = 1.5\ \text{V}\ (V_{VDD} < 4.0\ \text{V})$$

$$V_B = 2.5\ \text{V}\ (V_{VDD} > 4.0\ \text{V})$$

The V_{LDR} and V_{SFB} voltages are limited by the power supply voltage with the upper limit of V_{VDD} and the lower limit of 0 V.

EVALUATION BOARD SCHEMATICS AND ARTWORK

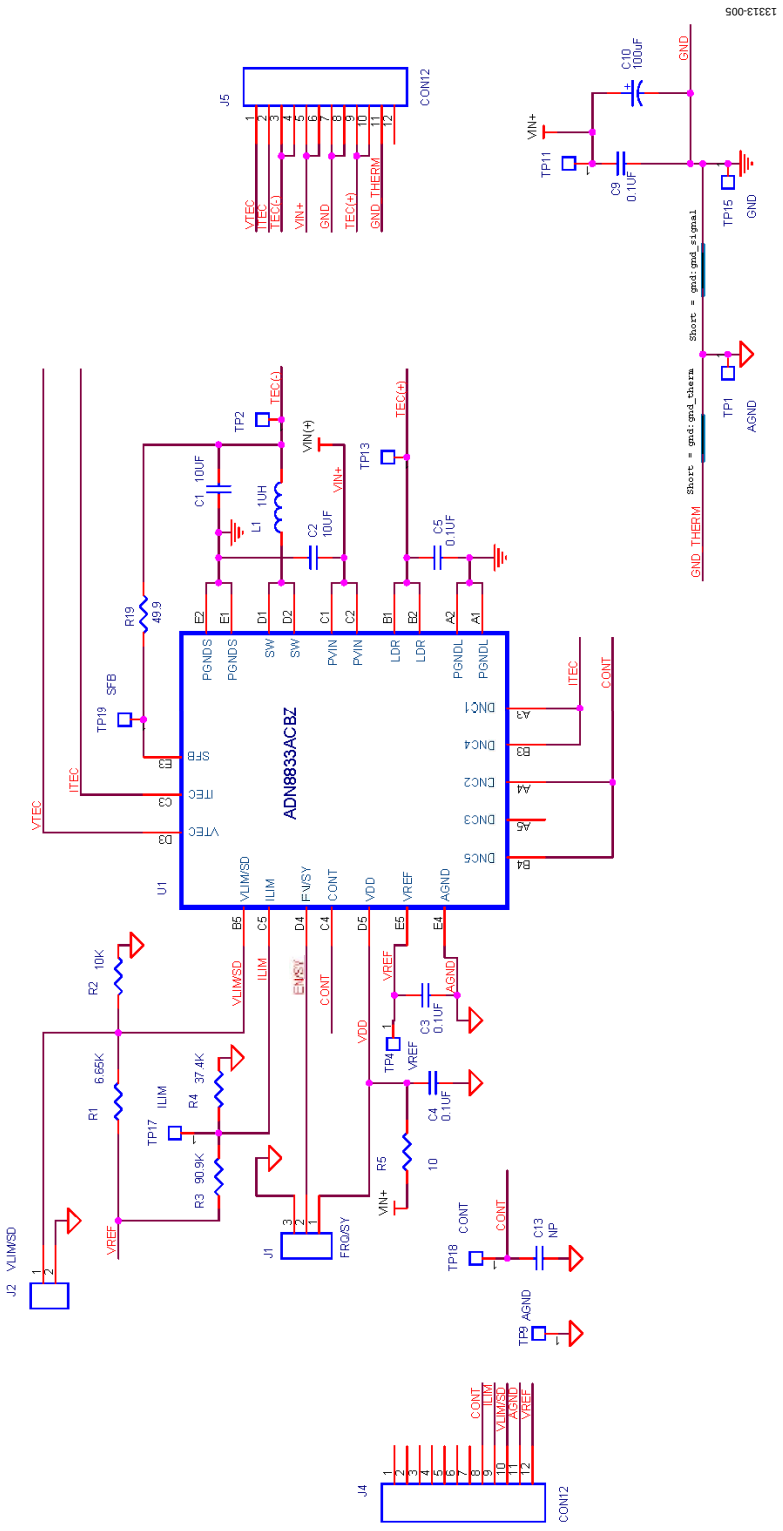

Figure 5. ADN8833CB-EVALZ WLCSP Evaluation Board Schematic

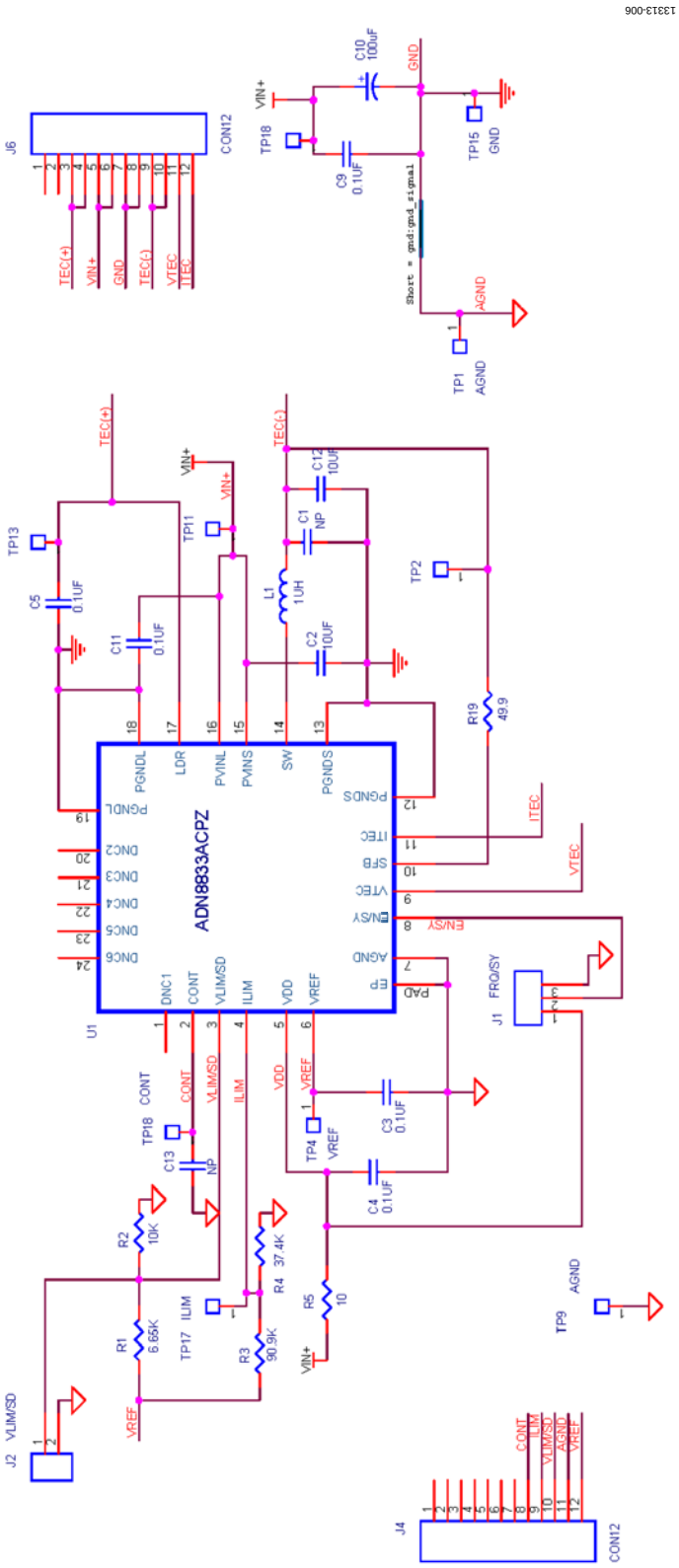

Figure 6. ADN8833CP-EVALZ LFCSP Evaluation Board Schematic

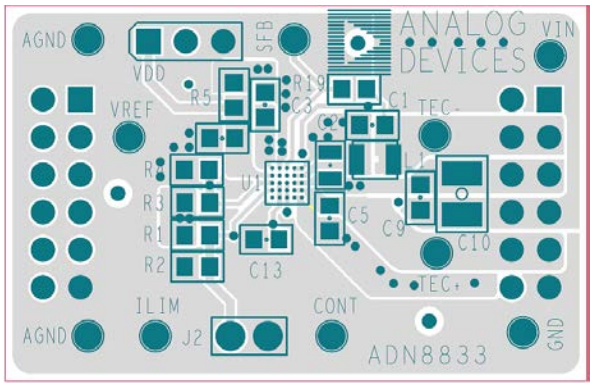

Figure 7. ADN8833CB-EVALZ Evaluation Board Top Layer

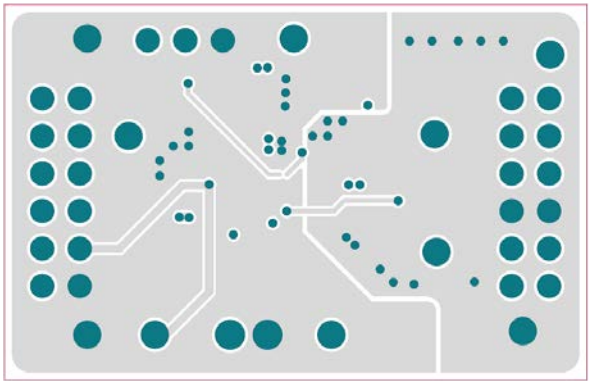

Figure 9. ADN8833CB-EVALZ Evaluation Board Second Layer

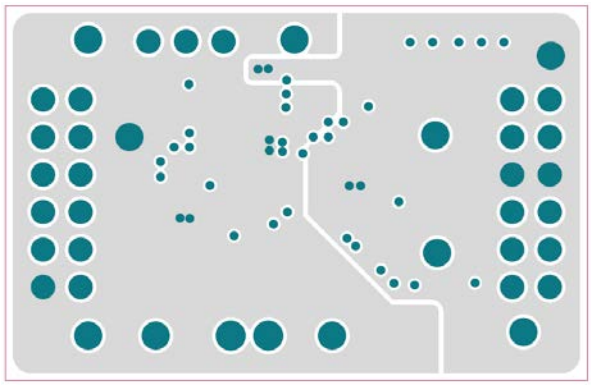

Figure 8. ADN8833CB-EVALZ Evaluation Board Third Layer

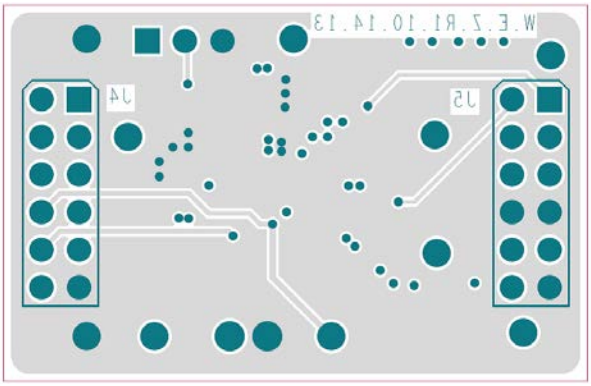

Figure 10. ADN8833CB-EVALZ Evaluation Board Bottom Layer

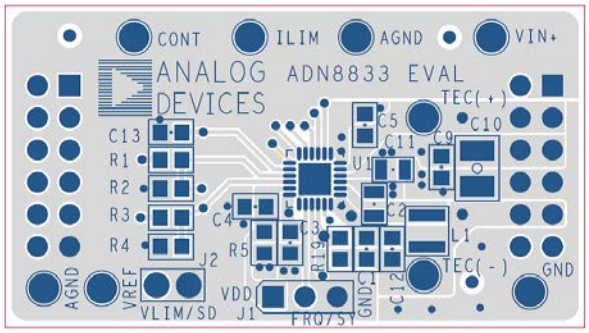

Figure 11. ADN8833CP-EVALZ Evaluation Board Top Layer

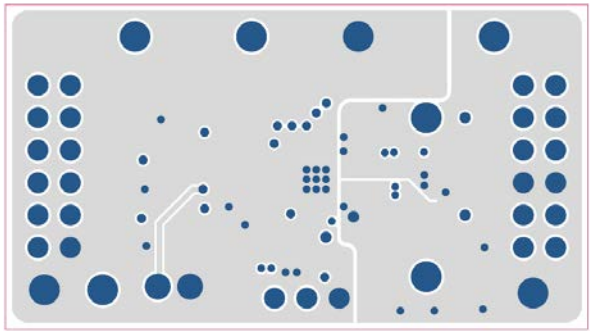

Figure 12. ADN8833CP-EVALZ Evaluation Board Second Layer

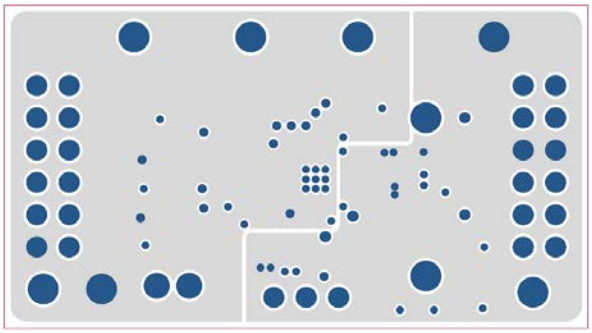

Figure 13. ADN8833CP-EVALZ Evaluation Board Third Layer

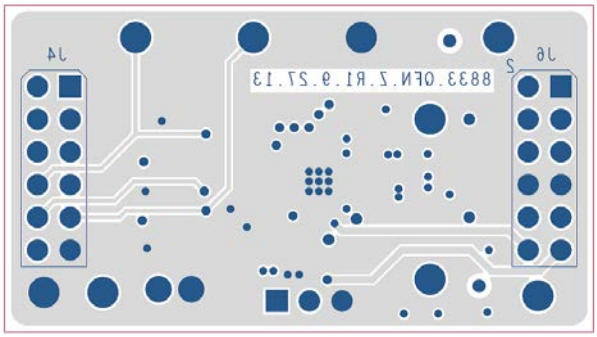

Figure 14. ADN8833CP-EVALZ Evaluation Board Bottom Layer

ORDERING INFORMATION

BILL OF MATERIALS

Table 4. ADN8833CB-EVALZ WLCSP Evaluation Board

Quantity	Reference	Description	Manufacturer	Part Number
2	C1, C2	Ceramic capacitor, 10 µF, 10 V, 10%, X7R, 0805	Taiyo Yuden	LMK212B7106KG-TD
4	C3, C4, C5, C9	Ceramic capacitor, 0.1 µF, 10 V, 10%, X7R, 0603	Kemet	C0603C104K8RACTU
1	C10	Tantalum capacitor, 100 µF, 6.3 V, 20%, 1411	Vishay	293D107X96R3B2TE3
1	J1	Jumper, 3-pin	Samtec	TSW-103-08-G-S
1	J2	Jumper, 2-pin	Samtec	TSW-103-08-G-S
2	J4, J5	Connector, double row, male, 12-pin	Samtec	TSW-112-08-G-D
1	L1	Inductor, 1 µH	TOKO	1286AS-H-1R0M
1	R1	Resistor, 6.65 kΩ, 1/10 W, 1%, 0603, SMD	Vishay	CRCW06036K65FKEA
1	R2	Resistor, 10 kΩ, 1/10 W, 1%, 0603, SMD	Vishay	ERJ-3EKF1002V
1	R3	Resistor, 90.9 kΩ, 1/10 W, 1%, 0603, SMD	Vishay	CRCW060390K9FKEA
1	R4	Resistor, 37.4 kΩ, 1/10 W, 1%, 0603, SMD	Vishay	CRCW060337K4FKEA
1	R5	Resistor, 10.0 Ω, 1/10 W, 1%, 0603, SMD	Vishay	CRCW060310R0FKEA
1	R19	Resistor, 49.9 Ω, 1/10 W, 1%, 0603, SMD	Vishay	CRCW060349R9FKEA
8	TP1, TP4, TP9, TP11, TP15, TP17, TP18, TP19	Test point	Samtec	TSW-103-08-G-S
1	U1	Ultracompact, 1 A, TEC driver, WLCSP package	Analog Devices, Inc.	ADN8833ACBZ-R7

Table 5. ADN8833CP-EVALZ LFCSP Evaluation Board

Quantity	Reference	Description	Manufacturer	Part Number
2	C2, C12	Ceramic capacitor, 10 µF, 10 V, 10%, X7R, 0805	Taiyo Yuden	LMK212B7106KG-TD
5	C3, C4, C5, C9, C11	Ceramic capacitor, 0.1 µF, 10 V, 10%, X7R, 0603	Kemet	C0603C104K8RACTU
1	C10	Tantalum capacitor, 100 µF, 6.3 V, 20%, 1411	Vishay	293D107X06R3B2T
1	J1	Jumper, 3-pin	Samtec	TSW-103-08-G-S
1	J2	Jumper, 2-pin	Samtec	TSW-103-08-G-S
2	J4, J6	Connector, male, 12-pin	Samtec	TSW-112-08-G-D
1	L1	Inductor, 1 µH	Coilcraft	XFL3012-102ME
1	R1	Resistor, 6.65 kΩ, 1/10 W, 1%, 0603, SMD	Vishay	CRCW06036K65FKEA
1	R2	Resistor, 10 kΩ, 1/10 W, 1%, 0603, SMD	Vishay	ERJ-3EKF1002V
1	R3	Resistor, 90.9 kΩ, 1/10 W, 1%, 0603, SMD	Vishay	CRCW060390K9FKEA
1	R4	Resistor, 37.4 kΩ, 1/10 W, 1%, 0603, SMD	Vishay	CRCW060337K4FKEA
1	R5	Resistor, 10.0 Ω, 1/10 W, 1%, 0603, SMD	Vishay	CRCW060310R0FKEA
1	R19	Resistor, 49.9 Ω, 1/10 W, 1%, 0603, SMD	Vishay	CRCW060349R9FKEA
7	TP1, TP2, TP4, TP9, TP15, TP17, TP18	Test point	Keystone	5010
2	TP2, TP11	Connector	MILL-MAX	3102-2-00-21-00-08-0
1	U1	Ultracompact, 1 A, TEC driver, LFCSP package	Analog Devices	ADN8833ACPZ-R7

NOTES

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

UG13313-0-10/15(0)

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